known, based upon current law, current 4 that passes through transistor 44 is equal to the current flow 4a plus 4b.

[0017] Referring to Figure 3, there is shown a graph of voltage versus time of the control signal applied to the external pin and the voltage versus time as it is applied to two addressable lines 20(a and n): WLg (addressable line 20a which is good) and WLg (addressable line 20n which is defective). Initially, if the control signal applied to the external pin is of a pulse 70, both the good word line 20a and the defective word line 20n would show an increase in voltage 72. After the pulse 70 has been applied, and a period 74 of ground is applied, the voltage on the good word line 20a would remain at the peak at which its voltage had risen. However, the voltage on the defective word line 20n would begin to decay. When another voltage pulse 76 is applied on the external pin, the voltage on the good word line 20a would again rise. The voltage 78 on the defective word line 20n, however, would also rise but from a lower level. Therefore, the end voltage difference between the good word line 20a and the defective word line 20n would differ as shown by the right-hand side of the graph shown in Figure 3. This condition can be detected by one of two methods.

[0018] In a first method, the current mirror circuit 30 can be used to apply the voltage to one end 14 of each of the addressable lines 20. A probe is attached to the other end 16 of each of the addressable lines 20 and the voltage at the other end 16 is detected and that would be determinative of whether the addressable line 20 is good or is defective.

[0019] In a second method of the present invention, the voltage on the various addressable lines 20 is used to effectuate an operation to the memory cells 12 that are electrically connected to the addressable line 20. For example, as disclosed in U.S. Patent 5,029,130, a high voltage is applied to the word line to cause an erase of the floating gate of the memory cells 12 attached to the word line 20. Thus, initially, all of the memory cells 12 that are connected to the addressable line 20 in question would be first programmed. Subsequently, the method of the present invention would be used to cause a high voltage to be supplied to the addressable line 20. If the memory cells 12 electrically connected to the addressable line 20 that is being tested fails to be